In re Patent Application of:
SMYTH ET AL.
Serial No. **10/022,595**
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In the Claims:

Claims 1-28 (Cancelled).

29. (Currently amended) An electronic module comprising:

a low temperature co-fired ceramic (LTCC) substrate;

at least one capacitive structure embedded in said LTCC substrate comprising a pair of electrode layers, an inner dielectric layer between said pair of electrode layers, and at least one outer dielectric layer adjacent at least one of said electrode layers and opposite said inner dielectric layer, said at least one outer dielectric layer having a dielectric constant less than a dielectric constant of said inner dielectric layer; and

at least one electronic device mounted on said LTCC substrate and electrically connected to said at least one embedded capacitive structure~~.~~;

said at least one outer dielectric layer comprising respective at least one outer dielectric layers adjacent each of said electrode layers and opposite said inner dielectric layer, and each at least one outer dielectric layer comprising a first outer dielectric layer and a second outer dielectric layer between said first outer dielectric layer and a respective electrode layer;

said second outer dielectric layer having a greater dielectric constant than a dielectric constant of said first outer dielectric layer.

Claims 30-32 (cancelled).

33. (Currently amended) The electronic module of Claim ~~32~~ 29 wherein the dielectric constant of said first outer dielectric layer is in a range of about 7-10, and the dielectric constant of said second outer dielectric layer is in a range of about 11-17.

34. (Original) The electronic module of Claim 29 wherein said inner dielectric layer has a dielectric constant of greater than about 2000.

35. (Currently amended) The electronic module of Claim 29 wherein said LTCC substrate further comprises at least one signal trace adjacent ~~said~~ at least one of said outer dielectric ~~layer~~ layers.

36. (Currently amended) The electronic module of Claim 29 wherein said ~~at least one~~ outer dielectric ~~layer~~ layers and said inner dielectric layer each comprises less than about 15% by weight of glass.

37. (Currently amended) The electronic module of Claim 29 wherein said ~~at least one~~ outer dielectric ~~layer comprises~~ layers comprise at least one of CaO, MgO, ZrO_2, BaO, and SiO_2.

38. (Original) The electronic module of Claim 29 wherein said inner dielectric layer comprises $BaTiO_3$.

39. (Original) The electronic module of Claim 29 wherein said electrode layers comprise at least one of Ag, Au, and AgPd.

40. (Original) The electronic module of Claim 29 wherein said inner dielectric layer has a thickness of less than about 3 mils.

41. (Original) The electronic module of Claim 29 further comprising conductive vias for electrically connecting said at least one electronic device and said at least one embedded capacitive structure.

42. (Original) The electronic module of Claim 29 wherein said at least one capacitive structure has a capacitive density of greater than about 1000 pF/mm^2.